ABSTRACT OF THE DISCLOSURE

A method, apparatus, and system for implementing off-chip cache memory in dual-use static random access memory (SRAM) memory for network processors. An off-chip SRAM memory store is partitioned into a resizable cache region and general-purpose use region (i.e., conventional SRAM use). The cache region is used to store cached data corresponding to portions of data contained in a second off-chip memory store, such as a dynamic RAM (DRAM) memory store or an alternative type of memory store, such as a Rambus DRAM (RDRAM) memory store. An on-chip cache management controller is integrated on the network processor. Various cache management schemes are disclosed, including hardware-based cache tag arrays, memory-based cache tag arrays, content-addressable memory (CAM)-based cache management, and memory address-to-cache line lookup schemes. Under one scheme, multiple network processors are enabled to access shared SRAM and shared DRAM, wherein a portion of the shared SRAM is used as a cache for the shared DRAM.